# Linear Technology Magazine Circuit Collection, Volume 1 

Richard Markell, Editor

## INTRODUCTION

Over the past several years Linear Technology, the magazine, has come of age. From nothing, the publication has come into its own, as has its subscriber list. Many innovative circuits have seen the light of day in the pages of our now hallowed publication.

This Application Note is meant to consolidate the circuits from the first few years of the magazine in one place. Circuits herein range from laser diode driver circuits to data acquisition systems to a 50 W high efficiency switcher circuit. Enough said. I'll stand aside and let the authors explain their circuits.

## CIRCUIT INDEX

A to D Converters ..... 2
LTC1292: 12-BIT DATA ACQUISITION CIRCUITS ..... 2
Temperature-Measurement System ..... 2
Floating, 12-Bit Data Acquisition System ..... 2
Differential Temperature Measurement System ..... 2
MICROPOWER S08 PACKAGED ADC CIRCUITS ..... 4
Floating 8-Bit Data Acquisition System ..... 4
$0^{\circ} \mathrm{C}-70^{\circ} \mathrm{C}$ Thermometer ..... 5
Interface ..... 6
LOW DROPOUT REGULATOR SIMPLIFIES ACTIVE SCSI TERMINATORS ..... 6
Power ..... 7
LT1110 SUPPLIES 6 VOLTS AT 550mA FROM 2 AA NiCAD CELLS ..... 7
50 WATT HIGH EFFICIENCY SWITCHER ..... 9
Filters ..... 10
CASCADED 8TH-ORDER BUTTERWORTH FILTERS PROVIDE STEEP ROLL-OFF LOWPASS FILTER ..... 10
DC-ACCURATE, PROGRAMMABLE-CUTOFF, FIFTH-ORDER BUTTERWORTH LOWPASS FILTER REQUIRES NO ON-BOARD CLOCK ..... 11
Miscellaneous Circuits ..... 12
A SINGLE CELL LASER DIODE DRIVER USING THE LT1110 ..... 12
LT1109 GENERATES VPP FOR FLASH MEMORY ..... 13
RF LEVELING LOOP ..... 13
HIGH ACCURACY INSTRUMENTATION AMPLIFIER ..... 14
A FAST, LINEAR, HIGH CURRENT LINE DRIVER ..... 15

## Application Note 52

## A to D Converters

LTC1292: 12-BIT DATA ACQUISITION CIRCUITS by Sammy Lum

## Temperature-Measurement System

The circuit in Figure 1 shows how a transducer output, such as a platinum RTD bridge, can be digitized with one op amp. This circuit is a modification of that found in Application Note 43. ${ }^{1}$ The differential input of the LTC1292 removes the common mode voltage. The LT1006 is used for amplification. The resistor tied between the + input of the LT1006 and the +IN input of the LTC1292 is to compensate for the loading of the bridge by resistor $\mathrm{R}_{\mathrm{s}}$. Full scale can be adjusted by the $500 \mathrm{k} \Omega$ trim pot and offset can be adjusted by the $100 \Omega$ trim pot in series with $R_{S}$. A lower RPLAT value than that in AN43 is used here to improve dynamic range. The signal voltage on the +IN pin must not exceed $V_{\text {REF }}$. The differential voltage range is $V_{\text {REF }}$ minus approximately 100 mV . This is enough range to measure $0^{\circ} \mathrm{C}$ to $400^{\circ} \mathrm{C}$ with $0.1^{\circ} \mathrm{C}$ resolution.

## Floating, 12-Bit Data Acquisition System

The circuit in Figure 2 demonstrates how to float the LTC1292 to make a differential measurement. This circuit will digitize a 5 V range from 10 V to 15 V with 12 bits of

[^0]resolution. The digital I/O has been level translated. The LT1019-5 is used in shunt mode to create the floating analog ground for the LTC1292. The digital I/O lines make use of 4.3V Zeners to clamp the single-transistor inverters. Opto-isolators can also be used. The floating analog ground should be laid out as a ground plane for the LTC1292. The $47 \mu \mathrm{~F}$ bypass capacitor should be tied from the $V_{\text {CC }}$ pin to the floating ground plane with minimum lead length and placed as close to the device as possible. Likewise, keep the lead length from the GND pin to the floating ground plane at a minimum (a low-profile socket is acceptable).

## Differential Temperature Measurement System

The circuit in Figure 3 digitizes the difference in temperature between two locations. The two LM134s are used as temperature sensors. These are ideally suited for remote applications because they are current output devices. This allows long wires to run from the sensor back to the LTC1292 without any degradation to the signal from the sensor. Resistor R ${ }_{\text {SET }}$ sets the current to $1 \mu \mathrm{~A} /{ }^{\circ} \mathrm{K}$. The current is converted to a voltage by the resistor R1 connected from $\mathrm{V}^{-}$to ground. The reference voltage and resistor were selected to give a change of $0.05^{\circ} \mathrm{C} / \mathrm{LSB}$. The resolution is given by ${ }^{\circ} \mathrm{C} / \mathrm{LSB}=\mathrm{V}_{\mathrm{REF}} /((4096)(1 \mathrm{~mA})(\mathrm{R} 1))$. The maximum temperature at each input is $125^{\circ} \mathrm{C}$. Note


Figure $1.0^{\circ}$ to $400^{\circ} \mathrm{C}$ Temperature-Measurement System

## Application Note 52

that if the temperature on the +IN pin is less than the temperature on the -IN pin, the output will be zero. Because the LTC1292 is being driven from a high source impedance, you should limit the CLK frequency to 100 kHz or less.

The software code for interfacing the LTC1292 to the Motorola MC68HC11 or the Intel 8051 is found in the LTC1292 data sheet. The code needs to be modified for the circuit in Figure 2 to account for the inversion introduced by the digital level translators.


Figure 2. Floating, 12-Bit Data Acquisition System


Figure 3. Differential Temperature-Measurement System

## Application Note 52

MICROPOWER SO8 PACKAGED ADC CIRCUITS
by William Rempfer

## Floating 8-Bit Data Acquisition System

Figure 4 shows a floating system that sends data to a grounded host system. The floating circuitry is isolated by two opto-isolators and powered by a simple capacitordiode charge pump. The system has very low power requirements because the LTC1096 shuts down between conversions and the opto-isolators draw power only when
data is being transferred. The system consumes only $50 \mu \mathrm{~A}$ at a sample rate of 10 Hz ( 1 ms on-time and 99 ms offtime). This is easily within the current supplied by the charge pump running at 5 MHz . If a truly isolated system is required, the system's low power simplifies generating an isolated supply or powering the system from a battery.


AN52•TA04

Figure 4. Power for this Floating ADC System is Provided by a Simple Capacitor-Diode Charge Pump. The Two Opto-Isolators Draw No Current Between Samples, Turning on Only to Send the Clock and Receive Data

## Application Note 52

## $0^{\circ} \mathrm{C}-70^{\circ} \mathrm{C}$ Thermometer

Figure 5 shows a temperature-measurement system. The LTC1096 is connected directly to the low cost silicon temperature sensor. The voltage applied to the $V_{\text {REF }}$ pin adjusts the full scale of the ADC to the output range of the sensor. The zero point of the converter is matched to the zero output voltage of the sensor by the voltage on the LTC1096's negative input.

Operating the ADC directly off batteries can eliminate the space taken by a voltage regulator. Connecting the ADC directly to sensors can eliminate op amps and gain stages. The LTC1096/LTC1098 can operate with small, $0.1 \mu \mathrm{~F}$ or $0.01 \mu \mathrm{~F}$ chip bypass capacitors.

Figure 6 shows the operating sequence of the LTC1096. The converter draws power when the $\overline{C S}$ pin is low and shuts itself down when that pin is high. In systems that convert continuously, the LTC1096/LTC1098 will draw its normal operating power continuously. A $10 \mu \mathrm{~s}$ wake up time must be provided to the LTC1096 after each falling $\overline{C S}$.

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{C S}$ low time. Bringing $\overline{\mathrm{CS}}$ low, waiting $10 \mu \mathrm{~s}$ for the wake up time, transferring data as quickly as possible, and then bringing it back high will result in the lowest current drain.


Figure 5. The LTC1096's High-Impedance Input Connects Directly to this Temperature Sensor, Eliminating Signal Conditioning Circuitry in this $0^{\circ} \mathrm{C}-70^{\circ} \mathrm{C}$ Thermometer


Figure 6. The ADC's Power Consumption Drops to Zero When CS Goes High. 10 1 s After CS Goes Low, the ADC is Ready to Convert. For Minimum Power Consumption Keep CS High for as Much Time as Possible Between Conversions

## Application Note 52

## Interface

## LOW DROPOUT REGULATOR SIMPLIFIES ACTIVE SCSI

 TERMINATORSby Sean Gold

The circuit shown in Figure 7 uses an LT1117 low dropout three terminal regulator to control the terminator's local logic supply. The LT1117's line regulation makes the output immune to variations in TERMPWR. After accounting for resistor tolerances and variations in the LT1117's reference voltage, the absolute variation in the 2.85 V output is only 4\% over temperature. When the regulator drops out at TERMPWR-2.85, or 1.25 V , the output linearly tracks the input with a 1V/V slope. The regulator provides effective signal termination because the $110 \Omega$ series resistor closely matches the transmission line's charac-
teristic impedance, and the regulator provides a good AC ground.

In contrast to a passive terminator, two LT1117s require half as many termination resistors, and operate at $1 / 15$ the quiescent current or 20 mA . At these power levels, PC traces provide adequate heat sinking for the LT1117's SOT-223 package. Beyond solving basic signal conditioning problems, this LT1117 terminator handles fault conditions with short circuit current limiting, thermal shutdown, and on-chip ESD protection.


Figure 7. SCSI Active Termination

## Application Note 52

## Power

## LT1110 SUPPLIES 6 VOLTS AT 550mA

## FROM 2 AA NiCAD CELLS

## by Steve Pietkiewicz

The LT1110 micropower DC-DC converter can provide 5V at 150 mA when operating from two AA alkaline cells. The internal switch $\mathrm{V}_{\text {CE(SAT) }}$ sets this power limit. Even with an external low drop switch, more power is not realistically possible. The internal impedance (typically $200 \mathrm{~m} \Omega$ fresh and $500 \mathrm{~m} \Omega$ at end-of-life) of alkaline AA cells limits peak obtainable battery power. Conversely, nickel-cadmium cells have a constant internal impedance ( $35 \mathrm{~m} \Omega-50 \mathrm{~m} \Omega$ ) for AA size) that increases only when the cell is completely
discharged. This allows power to be drawn from the cell at a far greater rate. The circuit in Figure 8 uses two AA NiCad cells to supply 6 volts at 550 mA . The circuit, developed for pagers with transmit capability, runs at full output current for 15 minutes with two Gates Millennium AA NiCad cells. With a 250 mA load, the circuit runs for 36 minutes (see Figure 9). Less heat is generated with a reduced load, resulting in the watt-hour difference observable above.


Figure 8. Schematic Diagram, 2 AA NiCad to $\mathbf{+ 6}$ Volt Converter


Figure 9. Operating Time at $\mathrm{I}_{\mathrm{LOAD}}=550 \mathrm{~mA}$ and 250 mA

The circuit uses a micropower LT1110 switchingregulator IC as a controller. The internal switch of the LT1110 furnishes base drive to $Q 1$ through the $220 \Omega$ resistors. Q1, in turn, supplies base drive to the power switch Q2. The Zetex ZTX849 NPN device is rated at 5A current and comes in a TO-92 package. For surface-mount fans, the FZT-849, also from Zetex, provides the same performance in an SOT-223 package. The $16 \Omega$ resistor provides a turn off path for Q2's stored charge. When Q2 is on, current builds in L1. As Q2 turns off, its collector flies positive until D1 turns on. L1's built-up current discharges through D 1 into C 2 and the load. The voltage at $\mathrm{V}_{\text {Out }}$ is divided by R4 and R3 and fed back into the FB pin of the LT1110, which controls Q2's cycling action. Switch current limit, which is necessary to ensure saturation over supply variations, is implemented by Q3-Q5. Q3, C1, R2, and the auxiliary gain block inside the LT1110, form a 220 mV reference point at the LT1110's SET pin. Transistors Q4 and Q5 form a common-base differential amplifier.

Q5's emitter monitors the voltage across $50 \mathrm{~m} \Omega$ resistor R1. When the voltage across R1 exceeds 220 mV , Q4 turns on hard, pulling current through R5. When the voltage at the LIM pin of the LT1110 reaches a diode drop below the $\mathrm{V}_{\text {IN }}$ pin, the internal switch turns off. Thus, maximum switch current is maintained at $220 \mathrm{mV} / 50 \mathrm{~m} \Omega$, or 4.4 A , over input variations and manufacturing spread in the LT1110's on time and frequency.

The circuit's output ripple measures 200 mV p-p, and efficiency is $78 \%$ at full load with a 2.4 V input. Output power can be scaled down for less demanding requirements. To reduce peak current, increase the value of R1. A $100 \mathrm{~m} \Omega$ resistor will limit current to 2.2A. L1 should be increased in value linearly as current is reduced. For a current limit of $2.2 \mathrm{~A}, \mathrm{~L} 1$ should be $10 \mu \mathrm{H}$. Base drive for Q 2 can also be reduced by increasing the value of the $10 \Omega$ resistor. These lower peak currents are much easier on alkaline cells and will dramatically increase alkaline battery life.

## Application Note 52

## 50 WATT HIGH EFFICIENCY SWITCHER

by Milton Wilcox

The high efficiency 10A step-down (buck) switching regulator shown in Figure 10 illustrates how different sized MOSFETs can be driven by the LT1158 without having to worry about shoot-through currents. Since 24 V is being dropped down to 5 V , the duty cycle for the switch (top MOSFET) is only $5 / 24$ or $21 \%$. This means that the bottom MOSFET will dominate the $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ efficiency losses, because it is turned on nearly four times as long as the top. Therefore a smaller MOSFET is used on the top, and the bottom MOSFET is doubled up, all without having to worry about dead time.

The LT1158 uses an adaptive system that maintains dead time independent of the type, the size, and even the number of MOSFETs being driven. It does this by monitoring the gate turn-off to see that it has fully discharged before allowing the opposite MOSFET to turn on. During turn-on, the hold-off capability of the opposing driver is boosted to prevent transient shoot-through. In this way, cross-conduction is completely eliminated as a design constraint.

The non-critical Schottky diode across the bottom MOSFETs reduces reverse-recovery losses. Figure 11 shows the operating efficiency for the Figure 10 circuit.

Switching regulator applications can take advantage of an important protection feature of the LT1158: remote fault sensing. By sensing the current on the output side of the inductor and returning the LT1158 fault pin to the PWM soft-start pin, a true current-mode loop is formed. The Figure 10 circuit regulates maximum current in the inductorto 15A with no output voltage overshoot upon recovery from a short circuit.


Figure 11. Operating Efficiency for Figure 10 Circuit. Current Limit is Set at 15A


Figure 10. 50W High Efficiency Switching Regulator Illustrates the Design Ease Afforded by Adaptive Dead Time Generation

## Application Note 52

## Filters

## CASCADED 8TH-ORDER BUTTERWORTH FILTERS PROVIDE STEEP ROLL-OFF LOWPASS FILTER by Philip Karantzalis and Richard Markell

Sometimes a design requires a filter that exceeds the specifications of the standard "dash-number" filter. In this case, the requirement was a low-distortion (-70dB) filter with roll-off faster than that of an 8th-order Butterworth. An elliptic filter was ruled out because its distortion specifications are too high. Two low power LTC1164-5s were wired in cascade to investigate the specifications that could be achieved with this architecture. The LTC1164-5
is a low power ( 4 milliamperes with $\pm 5$ volt supplies), clock-tunable, 8th-order filter, which can be configured for a Butterworth or Bessel response by strapping a pin. Figure 12 shows the schematic diagram of the two-filter system. The frequency response is shown in Figure 13, where it can be seen that the filter's attenuation is 80 dB at 2.3 times the cutoff frequency. The distortion, as shown in Figure 14 , is nothing less than spectacular. From 100 Hz to 1 kHz , the two filters have less than -74 dB distortion specifications. At the standard measurement frequency of 1 kHz , the specification is -78 dB .


Figure 12. Schematic Diagram: Low Power, 16th-Order Lowpass Filter (Two 8th-Order Butterworths Cascaded)


Figure 13. Frequency Response for fcLK $=\mathbf{2 0 k H z}$


Figure 14. Distortion Performance: Two LTC1164-5s, $\mathrm{f}_{\text {CLK }}=60 \mathrm{kHz}$ (57:1) Pin 10 Connected to $\mathrm{V}_{+}$

## Application Note 52

DC-ACCURATE, PROGRAMMABLE-CUTOFF, FIFTH-ORDER BUTTERWORTH LOWPASS FILTER REQUIRES NO ON-BOARD CLOCK
by Richard Markell
The new LTC1063 is a clock-tunable, monolithic filter with low-DC output offset ( 1 mV typical with $\pm 5 \mathrm{~V}$ supplies). The frequency response of the filter closely approximates a fifth-order Butterworth polynomial.

Most users choose to tune the filter with an on-board microprocessor and/or timer. This is quite convenient if these components are available. If a clock is not available, the LTC1063 can be tuned with an external resistor and capacitor. The scheme shown here allows the filter's cutoff frequency to be programmed using an external microprocessor or the parallel port of a personal computer. This allows the cutoff frequency of the filter to be set before the product is shipped.


Figure 15. Schematic Diagram of LTC1063 with Programmable Cutoff Frequency

## Application Note 52

The tuning scheme makes use of non-volatile, tunable capacitors available from Hughes Semiconductor. These capacitors allow approximately a decade of tuning range. More range could be obtained by using dual devices. Figure 15 shows the schematic diagram of the application. Be sure to place the variable capacitor as close as possible to the LTC1063 to minimize parasitic elements. Figure 16 shows the frequency response of the filter when the capacitor is varied from minimum to half-value, and then to maximum capacitance. The programming part of the circuit may be disconnected once the variable capacitor is set. The capacitor will remember its value until it is reprogrammed.

## Miscellaneous Circuits

## A SINGLE CELL LASER DIODE DRIVER <br> USING THE LT1110

## by Steve Pietkiewicz

Recently available visible lasers can be operated from 1.5 V supplies, given appropriate drive circuits. Because these lasers are exceptionally sensitive to overdrive, power to the laser must be carefully controlled lest it be damaged. Over-currents as brief as 2 microseconds can cause damage. In the circuit of Figure 17, an LT1110 switching regulator
serves as the controller within the single cell powered
laser diode driver. The LT1110 regulator is a high speed
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LT1073 LT1073.

The LT1110 is used here as an FM controller, driving a PNP power switch Q2, with a typical "ON" time of 1.5


Figure 16. LTC1063 Frequency Response
microseconds. Current in L 1 reaches a peak value of about 1.0A. The output capacitor C 2 has been specified for low ESR, and should not be substituted (damage to the laser diode may result).

The Gain Block output of the LT1110 functions with Q1 as an error amplifier. The differential inputs compare the photodiode current developed as a voltage across R2 to the 212 mV reference. The amplifier drives Q1, which modulates current into the I LIM pin. This varies oscillator frequency to control average current.

Overall frequency compensation is provided by R1 and C1, values carefully chosen to eliminate power-up overshoot. The value of current sense resistor R2 determines the laser diode power, as shown the 1000 ohms results in about a 0.8 milliwatt output.


Figure 17. LT1110 Laser Diode Driver Operating from a Single Cell

## Application Note 52

## LT1109 GENERATES VPP FOR FLASH MEMORY

by Steve Pietkiewicz

Flash memory chips such as the Intel 28F020 2Megabit device require a VPP program supply of 12 volts at 30 mA . A DC-DC converter may be used to generate 12 volts from the 5 volt logic supply. The converter must be physically small, available in surface-mount packaging, and have logic-controlled shutdown. Additionally, the converter must have carefully controlled rise time and zero overshoot. VPP excursions beyond 14 volts for $20 n$ or longer will destroy the ETOX²-process based device.


* 8-PIN PACKAGE ONLY
${ }^{\dagger}$ L1 $=$ COILTRONICS CTX 33-1 OR SUMIDA CD54-330 COILTRONICS (305) 781-8900 SUMIDA (708) 956-0666 AN52-TA18

Figure 18. All Surface Mount Flash Memory VPP Generator
Figure 18's circuit is well suited for providing VPP power for single or multiple flash memory chips. All associated components, including the inductor, are surface mount

[^1]devices. The SHUTDOWN input turns off the converter, reducing quiescent current to $300 \mu \mathrm{~A}$ when pulled to a logic 0. VPP rises in a controlled fashion, reaching 12 volts $\pm 5 \%$ in under 4 ms . Output voltage goes to $\mathrm{V}_{\text {CC }}$ minus a diode drop when the converter is in shutdown mode. This is an acceptable condition for Intel flash memories and does not harm the memory.

## RF LEVELING LOOP

by Jim Williams
Leveling loops are often a requirement for RF transmission systems. More often than not, low cost is more important than absolute accuracy. Figure 19 shows such a circuit.

The RF input is applied to A1, an LT1228 operational transconductance amplifier. A1's output feeds A2, the LT1228's current feedback amplifier. A2's output, the output of the circuit, is sampled by the A3-based gain control configuration. This arrangement closes a gain control loop back at A1. The 4pF capacitor compensates rectifier diode capacitance, enhancing output flatness vs frequency. A1's I SET $_{\text {input current controls its gain, allow- }}$ ing overall output level control. This approach to RF leveling is simple and inexpensive, and provides low output drift and distortion.


Figure 19. Simple RF Leveling Loop

## Application Note 52

## HIGH ACCURACY INSTRUMENTATION AMPLIFIER

by Dave Dwelley

The LTC1043 and the LTC1047 combine to make a high performance low frequency instumentation amplifier as shown in Figure 20. The LTC1043 switched capacitor block is configured as a sampling front end, providing exceptional CMRR and rail-to-rail input operation. Itworks by attaching a $1 \mu \mathrm{~F}$ capacitor across the two inputs, letting it charge to the input voltage. Once charged, the capacitor is disconnected from the input terminals and reconnected to the output terminals, where it transfers its charge to the $1 \mu \mathrm{~F}$ capacitor at the LTC1047's input. Any common mode voltage present at the inputs is subjected to a capacitive divider between the $1 \mu \mathrm{~F}$ flying cap and the IC's parasitic capacitance. With the LTC1043's parasitics typically below 1pF, this gives AC CMRR above 120dB. The analog switches in the LTC1043 are purely resistive, so they add no DC offset to the signal.

The output signal (with the common mode stripped off) is then amplified by the LTC1047, a precision, micropower zero-drift op amp. The LTC1047 amplifies the signal by the desired amount, adding less than $10 \mu \mathrm{~V}$ offset and $0.05 \mu \mathrm{~V} /$ ${ }^{\circ} \mathrm{C}$ drift. The sampling frequency of the LTC1043 with single 5 V supply is about 400 Hz , allowing differential signals below 200 Hz to be amplified with no aliasing. Note that common mode signals are not sampled; thus they will not alias regardless of frequency until the common mode/ differential mode signal ratio approaches 120dB! The entire system draws $60 \mu \mathrm{~A}$ with a single 5 V supply and provides two independent channels.


Figure 20. High Accuracy Instrumentation Amplifier

## A FAST, LINEAR, HIGH CURRENT LINE DRIVER by Walt Jung and Rich Markell

Among linear applications not usually seen are those which require high speed combined with either very low DC error, or high load current. Such applications can be solved by combining the best attributes of two ICs, either one of which may not be capable by itself of the entire requirement.

A case in point is the line driver of Figure 21, which uses an LT1122 JFET input op amp as the gain element combined with an LT1010 buffer. This provides the output current of the LT1010 (typically 150 mA ) but with the basic DC and low level AC characteristics of the LT1122. The circuit is capable of driving loads as low as $100 \Omega$ with very low distortion. The input referred DC error is the low DC offset of the LT1122, typically 0.5 mV or less. Large signal characteristics are also very good, due to the $80 \mathrm{~V} / \mu \mathrm{s}$ symmetrical SR of the LT1122.

The circuit as shown is configured as a precise gain of 5 non-inverting amplifier by gain set resistors R2 and R1, with the LT1010 unity gain voltage follower inside the overall feedback loop. This provides current buffering to the op amp, allowing it to operate most linearly. Small signal bandwidth is set by the time constant of R2 and C1, and is 1 MHz as shown, with a corresponding risetime of about 400ns.

Performance with $\pm 18 \mathrm{~V}$ supplies is shown in Figures 22a and 22 b , with output generally $5 \mathrm{~V}_{\text {RMS }}$ or equivalent, driving $100 \Omega$ directly. THD is shown in Figure 22a, with input level swept up to output clipping level, at a fixed 10 kHz frequency. The distortion is generally well below $0.01 \%$, and improves substantially for lower frequencies.


Figure 21. Line Driver

## Application Note 52

CCIF IM distortion performance of the circuit for similar loading is shown in Figure 22b, driving a load of $100 \Omega$ at a swept level, again up to output clipping. The LT1122 amplifier is represented by the lower of the two curves, with distortion around the $0.0001 \%$ level. Also shown for comparison in this plot is the distortion of a type 156 JFET op amp (also driving the LT1010 buffer with other conditions the same). The 156 op amp uses a design topology with an intrinsically asymmetric SR. This manifests itself


Figure 22a. THD vs Input Level
as rising even order distortion for methods such as this CCIF test. For this example, the distortion is more than an order of magnitude higher than that of the faster, symmetric slewing LT1122 for the same conditions.

Applications of this circuit include low offset linear buffers such as for $A / D$ inputs, line drivers for instrumentation use, and audio frequency range buffers such as very high quality headphone use.


Figure 22b. CCIF IM Distortion vs Input Level

Linear Technology, the magazine, is published 3 times a year.
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[^0]:    ${ }^{1}$ Williams, Jim, "Bridge Circuits, Marrying Gain and Balance," Application Note 43, Linear Technology Corp.

[^1]:    ${ }^{2} \mathrm{ETOX}$ is a trademark of Intel Corporation.

